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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,035	03/21/2001	Masanari Asano	024354-00001	2760

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EXAMINER	
WALLACE, SCOTT A	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,035	ASANO, MASANARI	
	Examiner	Art Unit	
	Scott Wallace	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8,9,11-13 and 15-19* is/are rejected.

7)☒ Claim(s) *3,4,7,10,14 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 12, 13, 15, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Aleksic et al., U.S. Patent No. 6,173,367.

4. As per claims 12 and 17, Aleksic et al discloses an image processing method comprising the steps of: setting up, in a storage circuit in which image data is stored (column 4 lines 48-65, cache), a range of an image area in which the image data is written (column 4 lines 48-65, 3D data) and a range of an additional area which is adjacent to the image area (fig 2 and column 6 lines 1-60) and in which data other than the image data is written (column 4 lines 48-65, Z-data), with information supplied to a memory space of said storage circuit as a parameter (column 3 lines 38-41); writing the additional data other than the image data from external into the additional area in said storage circuit according to a first write control signal (column 3 lines 50-68 and column 4 lines 48-65); writing the image data at an address location of the image area in said storage circuit according to a second write control signal (column 3 lines 50-68 and column 4 lines 48-65); and reading out the additional data stored in the additional area

and the image data stored in the image area in said storage circuit in response to a first read control signal (column 12 lines 40-68), wherein the additional data are written in with an address of the additional area (column 3 lines 50-68 and column 4 lines 48-65).

5. As per claim 13, Aleksic et al discloses wherein said step of reading out the additional data comprises the steps of: reading out the additional data from the additional area in said storage circuit in response to the first read control signal (column 3 lines 50-68 and column 4 lines 48-65); and reading out the image data from the image area in said storage circuit in response to a second read control signal (column 3 lines 50-68 and column 4 lines 48-65).

6. As per claim 15, Aleksic et al discloses wherein said step of reading out the additional data inserts the additional data read out from the additional area into a predetermined position of a video signal (column 1 lines 45-46 and column 3 lines 50-68 and column 4 lines 48-65).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2, 5-6, 8-9, 11, 16, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garrett et al., U.S. Patent No. 4,987,551 in view of Sawada et al., U.S. Patent No. 4,984,208.

9. As per claims 1 and 16, Garrett discloses an image processor (column 1 lines 10-16, cursor) comprising: a storage circuit storing therein image data (fig 2); a memory control circuit comprising an address generation circuit generating an address in said storage circuit to and from which the image data is written in and read out (column 4 lines 14-40), said memory control circuit comprising an area

adjustment circuit which sets up an additional area adjacent to an area in which the image data are actually stored in a memory space of said storage circuit (column 2 lines 57-68) and storing therein additional data other than the image data (column 2 lines 57-68, cursor data), which adjust the address generated by said address generation circuit (column 2 lines 57-68), and which reads out the image data from said storage circuit, including the additional data in the additional area (column 4 lines 29-40), in response to the address and a read control signal supplied to said storage circuit, wherein the additional data are written in with an address of the additional area (column 4 lines 14-40). However, Garrett does not disclose a data input/output circuit controlling input/output of the image data; an access control circuit controlling access of writing in and reading out the image data to and from said storage circuit; a refresh circuit controlling refreshing of said storage circuit. This is disclosed in Sawada et al in column 1 lines 9-25 and column 2 lines 54-59 and fig 1, #55. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an input/output control, an read/write control and a refresh control from the system of Sawada et al with the system of Garrett because Garrett uses a DRAM frame buffer as seen in column 3 lines 60-65 and Sawada et al uses these controls to write data without prolonging the period of the read/write cycle (column 2 lines 54-60). Therefore this would improve the DRAM of Garrett by not prolonging the period of the read/write cycle.

10. As per claim 2, Garrett et al discloses wherein said area adjustment circuit sets up the additional area immediately preceding or following the area in which the image data is stored (fig 2 column 2 lines 55-68).

11. As per claim 5, Garrett et al discloses wherein said area adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as a parameter (column 5 lines 8-45).

12. As per claim 6, Garrett et al discloses wherein said area adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as a parameter (column 5 lines 8-45).

13. As per claim 8, Garrett et al discloses wherein said area adjustment circuit supplies the additional data, which is read out from the additional area, to a predetermined position in a video signal (column 4 lines 29-40).

14. As per claim 9, Garrett et al discloses wherein said area adjustment circuit supplies the additional data, which is read out from the additional area, to a predetermined position in a video signal (column 4 lines 29-40).

15. As per claim 11, Garrett et al discloses wherein said access control circuit supplies the additional data other than the image data to said memory circuit (column 4 lines 14-40).

16. As per claims 18 and 19, Garrett et al discloses wherein said additional area has an adjustable width (column 5 lines 30-45).

Allowable Subject Matter

17. Claims 3-4, 7, 10, 14 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Wallace whose telephone number is 571-272-7652. The examiner can normally be reached on Mon-Fri 9-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott Wallace
Examiner
Art Unit 2675

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SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER